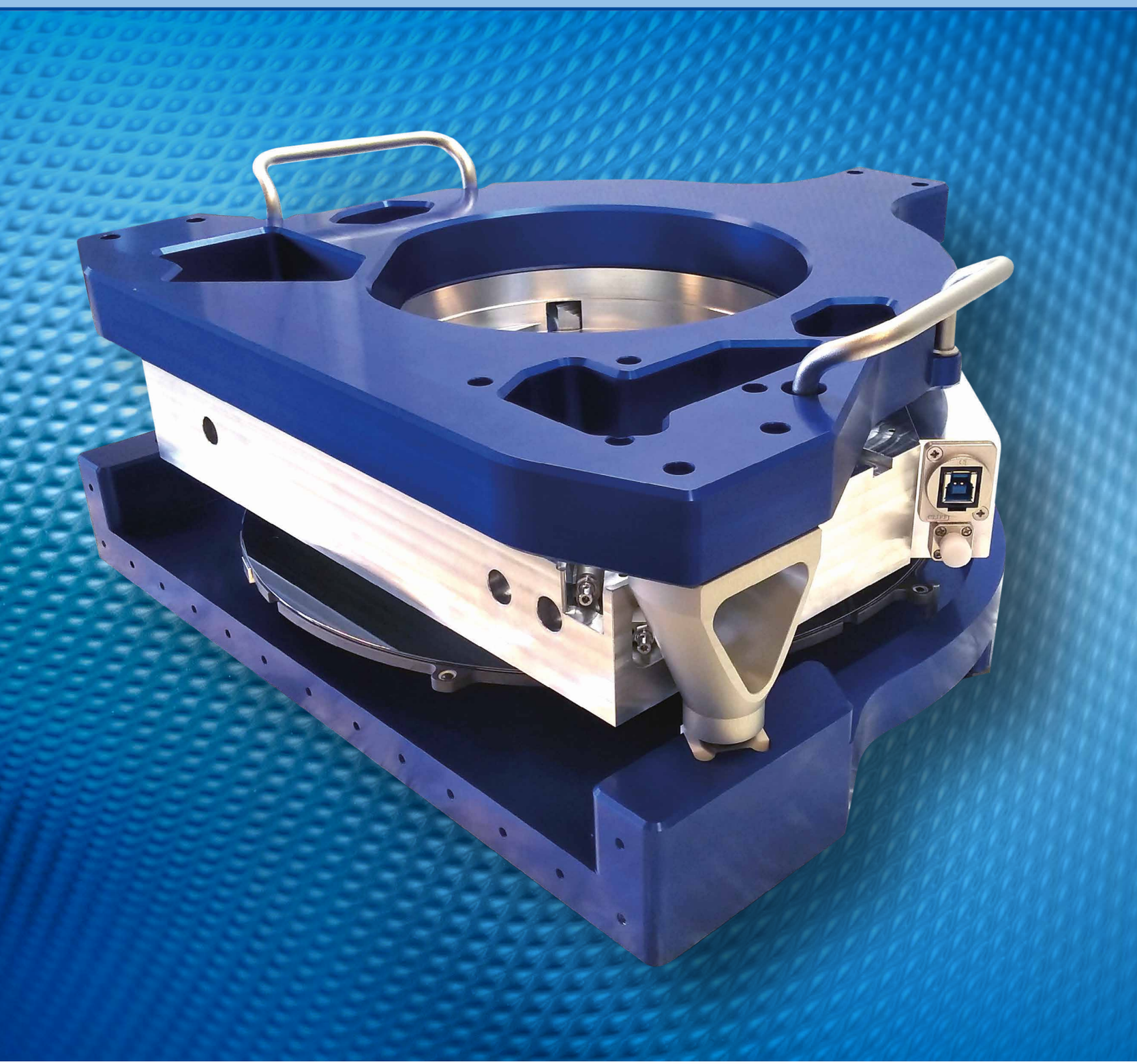
DSPE MIKRONIEK
2022 (VOL. 62) ISSUE 1
PROFESSIONAL JOURNAL ON PRECISION ENGINEERING



- THEME: HIGH-TECH SYSTEMS
- HIGH-NA EUVL THE NEXT MAJOR STEP IN LITHOGRAPHY
- TEACHING DESIGN PRINCIPLES AND MACHINE DYNAMICS
- WIM VAN DER HOEK'S BROAD VIEW

MIKRONIEK IS A PUBLICATION OF THE DUTCH SOCIETY FOR PRECISION ENGINEERING – WWW.DSPE.NL

PUBLICATION INFORMATION

Objective
Professional journal on precision engineering and the official organ of DSPE, the Dutch Society for Precision Engineering. Mikroniek provides current information about scientific, technical and business developments in the fields of precision engineering, mechatronics and optics. The journal is read by researchers and professionals in charge of the development and realisation of advanced precision machinery.

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Subscription
Mikroniek is for DSPE members only.
DSPE membership is open to institutes, companies, self-employed professionals and private persons, and starts at € 80.00 (excl. VAT) per year.

Mikroniek appears six times a year.

ISSN 0026-3699

The cover image (featuring the design of a level sensor for the semiconductor industry) is courtesy of Hittech Multin. Read the article on page 5 ff.

IN THIS ISSUE

THEME: HIGH-TECH SYSTEMS

FEATURES

IN ADDITION TO SYSTEMS ENGINEERS, MORE SYSTEMS THINKERS ARE NEEDED

We are facing major transformations. Look at the energy transformation needed to combat climate change. These kinds of major transformations require a more systemic approach. A change for the sake of our future and the future of our children. For those complex changes, you also need systems thinkers: non-technicians who look at the larger system, together with systems engineers and others. In the end, we all work on subsystems that are interconnected.

As a Brainport region, we are champions in systems engineering for high-precision equipment. Take ASML's lithography machine. The making of that machine consists of many subsystems that ingeniously have been brought together. As a systems thinker, I understand this way of thinking and its language.

Look at connected, coordinated and autonomous mobility. This promises to be a solution for the major mobility challenges. Yet, why is it often limited to initiatives at a small-scale level? I believe this is due to its complexity. Since it is not just the technology to make that car drive independently, but a whole sequence of links, including traffic systems, a charging infrastructure, a road structure, the vehicle and road users. Coordination of all those links also requires a systemic thinking approach.

With those major transformations, you see that there is no problem owner for the bigger, complex, but necessary system change. There are problem owners for the subsystems, but there is no one for the overall architecture. This is the independent role that we assume. Someone who takes care of the integration in existing systems like society. Without it, we will never take the big steps to realise autonomous driving, for example.

Take the Brainport region. Also a large ecosystem, with different interests. One has to bring these together to achieve a common goal. Thinking from a systems perspective, you look at how these interests relate to each other. On the one hand, you have technological solutions, on the other, you have social issues that also require a solution.

That is similar to what a systems engineer does. That role and responsibility determination at the front. As a non-technician, a systems thinker, you can also look at a system, and together we can create common knowledge, which makes it easier for us to place ourselves in the world of experience of the other. Without judgement.

Systems thinkers are not omniscient. As a systems thinker, I realise that we are part of a larger system. Our region is again a subsystem in the system of the Netherlands in the system of the world. A systems thinker is continuously open to connecting with another system. That's why our work is never finished. There is always new information coming in that we have to post again. Then it's back to the common ground and determining what needs to be adjusted to move forward. Always make it manageable and understandable for others.

Systems thinking, in my view, is a skill that we should be exposed to at a young age. Maybe even as a subject in primary school. It is necessary to be able to take on the major transformations in our increasingly complex world.

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AFFORDABLE STABILITY IN HEIGHT MEASUREMENT

In a proof-of-concept study, Hittech Multin successfully designed and built a cost-efficient level sensor, specifically aimed at semiconductor applications, using mostly off-the-shelf parts and a self-developed processing algorithm. The target measurement stability was 50 nm. Experiments on a 300-mm wafer showed a short-term instability between 6.4 nm and 10^2 nm, at the centre and the edge of the measurement range, respectively. The next research stage will focus on bringing stability performance within specification throughout the entire range. Finally, the sensor's ability to also measure wafer tilt (Rx and Ry), for counteracting tilt-dependent wafer height measurement errors, will be investigated.

THOMAS OOMS AND FRED COUWELEERS

Technical introduction

The most critical step in the fabrication of a computer chip is lithography. In this step, the pattern of the electric circuits is 'written' on a wafer. A lithography system essentially projects an (electron-) optical image onto a resist-coated wafer. (Note: exposure using either photons (light) or electron beams is possible.) The top surface of the wafer must be in the (electron-) optical focal plane throughout the exposure or else the written pattern will be blurred, which would result in a non-functioning chip. The axial range in which the image is sharp is called the depth-of-focus (*DOF*), which can be calculated using the expression:

$$DOF = \lambda / (2 \cdot NA^2)$$

Here, λ is the wavelength of the light used and *NA* is the numerical aperture at the image side of the (electron-) optical system [1]. Lithography systems of the deep-UV generation use light with a wavelength near 200 nm. To write patterns as small as possible, these systems have an *NA* as large as 1 [-]. The *DOF* is then approximately 100 nm.

Capacitive sensors are available commercially that have a resolution as small as a few nanometers [2]. It is therefore possible to measure and (with proper actuation) control the wafer height with sufficient precision. However, to avoid a volume conflict with the (electron-) optical column, these sensors must be outside this column. The height measurements done at those locations only lead to the correct height at the centre of the column when the wafer is sufficiently flat. An optical sensor can measure on the (electron-) optical axis. A sensing light beam can travel at an angle towards the (nominal) intersection of (electron-) optical axis and wafer top-surface, reflect and then travel to a detector at the other side of a level-sensor (LS) module (Figure 1).

We decided to include the development of a "Level Sensor for application in Semiconductor Industry" in our internal technology development programme. The aim was to design and build an optical level sensor based on low-coherence interferometry, using standard parts, that is capable of measuring wafer height changes of 50 nm (resolution), over a vertical range of 300 µm (peak-to-peak). It turned out that deriving the wafer height from the optical sensor signals (signal processing) is not a trivial task in the presence of noise and changes in signal shape related to wafer height.

AUTHORS' NOTE

Thomas Ooms holds a Ph.D. degree in Applied Physics (2008) from Delft University of Technology (NL). He has worked at Mapper Lithography and Hittech Multin, and currently works at ASML. His expertise is in the design of (optical) metrology solutions to accomplish accurate positioning in high-tech systems.
Fred Couweleers holds a Master's degree in Applied Physics (1990) from Eindhoven University of Technology (NL). He has worked predominantly in the field of (optical) metrology in industry and contract research organisations with a focus on production. Currently, he works as a senior optical designer at Hittech Multin on various optics projects, including microscopy, beam shaping and data merging.

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Hittech Group

Hittech Multin, located in Den Haag (NL), is part of the Hittech Group, which comprises nine companies in the Netherlands, Germany and Malaysia, and has a turnover of €140 million. Hittech is a first-tier system supplier in mechatronic and optical systems, and is active in the semicon, medical and lab equipment markets. The development group at Hittech Multin was responsible for the design and realisation of the level sensor within the framework of the "Sensors for Semicon" part of Hittech's Technology Program, under the supervision of Pieter Kappelhof, director Technology of the Hittech Group.

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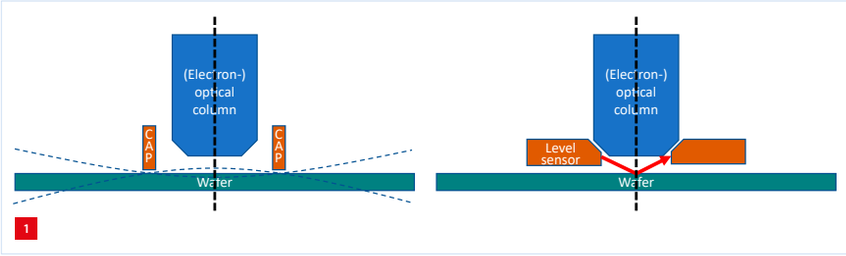


Off-axis measurement using capacitive sensors (left) versus on-axis measurement by an optical sensor (right).

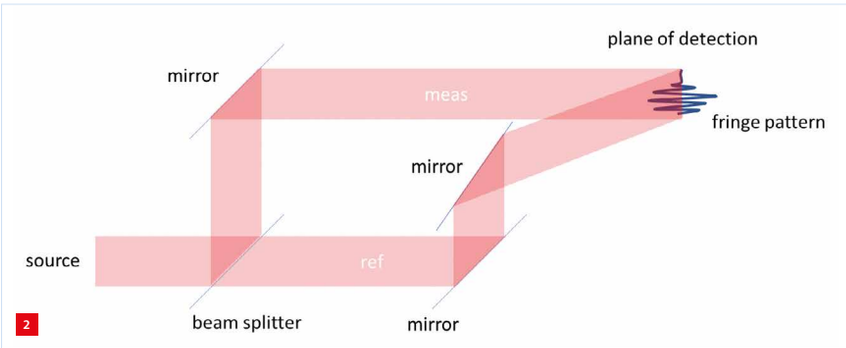
Concept design

To reach the required resolution, the sensor technology was based on interferometry. A single optical power measurement (one measurement using one photo-detector) is insufficient to generate a reliable height measurement, e.g. because the single power measurement would depend on the unknown wafer reflectivity. Instead, it is necessary to record a pattern with multiple fringes. This is realised by varying optical path length (*OPL*) within the interferometer.

The *OPL* can be varied as a function of time, for example by a scanning mirror in the reference branch. But the *OPL* can also be varied as a function of space, for example by letting the two interferometer beams combine at an angle onto a pixel-array sensor (camera) in a Mach Zehnder-like design (Figure 2). The second option was chosen so as to minimise the number of parts required and avoid having to generate small, but very reproducible, movements.

Although the typical light source for interferometry is a laser, such a highly coherent light source would result in a signal that is periodic over a large wafer-height range. In this case, it would be impossible to redetermine the wafer height after the measurement beam has been interrupted, for example during a wafer swap, because there is no way to tell how many fringes the signal has shifted after interruption with respect to the signal before interruption. To avoid this ambiguity, the sensor uses a low-coherent light source.

As the light source has low coherence, the fringe pattern will only appear where the *OPL* of the two interferometer beams



Layout of a Mach Zehnder-like interferometer.

is almost equal, as shown in Figure 3. When the wafer is at the bottom of its range, the measurement beam wavefront arrives 'late' at the detector, compared to the corresponding reference beam wavefront. The fringe pattern then forms near one edge of the detector. When the wafer is at the centre of its range, the fringe pattern forms at the centre of the detector. When the wafer is at the top of its range, the fringes form near the other side of the detector. See Figure 3.

The essence of data processing is to determine the position of the fringes on the detector. The wafer height $\tilde{Z}_{waf}$ can then be estimated by multiplying this position with a proportionality factor.

Detailed design

Hardware

After the measurement concept had been validated in a breadboard set-up, the detailed design of the LS prototype commenced. The LS prototype was designed to consist of two modules, an 'electronics box' and a 'ring'. The ambition was to use commercial off-the-shelf parts, apart from a custom part to position the optomechanical parts with respect to each other and to serve as an interface to the environment (e.g. the lithography tool).

The electronics box contains a low-coherent infrared light source (super luminescent diode, SLD [3]), which emits light through a polarisation-maintaining (PM) single-mode (SM) fibre. An 840 nm wavelength was chosen because the SLD with this wavelength has a particularly large bandwidth, which leads to a narrow interference pattern (i.e., with relatively few fringes; an *OPL* difference of 5.3 wavelengths reduces the fringe contrast by only 50%), which reduces the chance of making a height measurement error due to an *OPL* measurement error of one or more exact wavelengths. A laptop PC performs real-time data analysis and displays the results.

The ring receives light via a PM SM fibre. Inside the ring body, light is collimated and split into a measurement branch and a reference branch. Light in the measurement branch travels (via mirrors) to the wafer (angle of incidence *AOI* with respect to the normal is 68°), reflects and travels to a 'primary interference plane'. This large angle of incidence is derived from the volume claim in an earlier project and provides ample space for an (electron-) optical column in the centre of the ring. The change in *OPL* as a result of a change in wafer height is:

$$dOPL = 2 \cdot dZ \cdot \cos(AOI)$$

In this geometry, the result is: $dOPL = 0.75 \cdot dZ$.

NEXT MAJOR STEP IN LITHO – THE IMEC PERSPECTIVE

In the course of 2025, we expect to see the introduction of the first high-NA extreme ultraviolet (EUV) lithography equipment in high-volume manufacturing environments. These next-generation lithography systems will be key to advance Moore's Law towards the logic 2-nm technology generation and beyond. In this article, imec scientists and engineers involved in preparing this major next step in semiconductor lithography (driven by equipment maker ASML) discuss challenges and opportunities. They highlight recent insights and progress obtained in developing the patterning processes, metrology and photomasks needed for enabling the high-NA EUV lithography infrastructure.

DANILO DE SIMONE, GIAN LORUSSO, VICKY PHILIPSEN AND KURT RONSE

A leap in resolution

2019 marked an important milestone for extreme ultraviolet (EUV) lithography: ASML's EUV lithography systems were for the first time deployed in the mass production of logic chips of the 7-nm technology generation. Inserted to pattern the most critical layers of the chips' back-end-of-line, it enabled printing metal lines with pitches as tight as 36-40 nm.

With an extremely short wavelength of 13.5 nm, EUV lithography was introduced to succeed 193-nm (immersion) lithography as the most cost-effective manufacturing solution for the most advanced chip nodes. This transition was dictated by the Rayleigh equation for resolution: $R = k_1 \cdot \lambda / NA$, with k_1 a constant (process factor), λ the wavelength and *NA* the numerical aperture. According to this equation, the resolution of a lithography tool – and thus its ability to print features with a certain half pitch or critical dimension (*CD*) – can be improved by using light with smaller wavelength during wafer exposure. Moreover, the complex, expensive multiple-patterning requirements of 193 nm – which involve splitting a chip pattern into two or more simpler masks – could be moved back again to single-patterning EUV.

On the development side, researchers have been continuously trying to push further the single-print capability of today's most advanced EUV full-field scanner, ASML's NXE platform. Last year, for example, imec and ASML were able to demonstrate 28-nm-pitch single-exposure patterning readiness for lines/spaces, corresponding to critical back-end-of-line metal layers of a 5-nm logic technology node. This brings the current scanner close to its resolution limit for high-volume manufacturing, which is around 13 nm (26 nm pitch). Along with the evolution in logic, memory manufacturers are increasingly looking at using EUV lithography for meeting the high-density requirements for future memories – for example for patterning critical DRAM structures.

At the same time, multiple-patterning EUV lithography options are being explored to advance EUV to the next nodes. While these 'tricks' offer more relaxed pitches, they also come with a downside: an increased number of processing steps, adding to the cost, complexity and processing time of the patterning step.

2023 will mark a new milestone in the evolution of EUV lithography. By then, the first new generation of EUV lithography tools is expected to enter the scene: a high-NA EUV lithography scanner – projected to print the most critical features of 2-nm (and beyond) logic chips in a smaller number of patterning steps. The transition towards high-NA lithography is again justified by the Rayleigh equation, which provides a second knob for improving the resolution: increasing the *NA* of the projection lens. The *NA* controls the amount of light (more precisely, the number of diffraction orders) that is used to form the image, and thus controls the quality of the image.

Transitioning to higher-NA imaging equipment has been applied before, remember the move from 193-nm dry to 193-nm immersion lithography. At that time, the optical trick of replacing the air between lens and wafer with water allowed a 45% increase in *NA*. In the case of EUV, ASML will move from the current *NA* of 0.33 to 0.55 (i.e., a 67% increase) by redesigning the optics within the lithography system. 0.55NA EUV lithography promises to ultimately enable 8 nm resolution, corresponding to printing lines/spaces of 16 nm pitch in one single exposure.

AUTHORS' NOTE

All authors work at imec, a leading nanoelectronics research centre based in Flanders (B). Danilo De Simone is the principal staff member leading the research on patterning materials for EUV lithography, Gian Lorusso is a principal scientist working on EUV and metrology, Vicky Philipsen is a lithography engineer, and Kurt Ronse is the Advanced Patterning Program director. This article is a slightly abridged version of a longread that was published last October on the imec website.

www.imec-int.com/en/reading-room
www.imec-int.com/en/articles/high-na-euvl-next-major-step-lithography

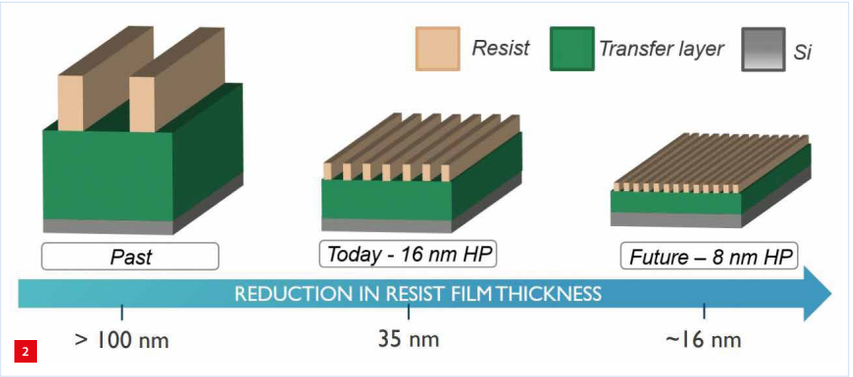
An ambitious timeline

0.55NA EUV lithography will push the patterning towards features smaller than what is possible with current 0.33NA EUV lithography systems. But the road forward is ambitious. The development of EUV lithography systems goes back to the 2000s, with a ten-year time span between the installation of the first pre-production EUV scanners and the recent introduction of EUV lithography in high-volume manufacturing. For high-NA, the ambition is to compress that time frame to only three years, with a first prototype (the EXE:5000; Figure 1) foreseen for 2023.

Rendering of ASML's EXE:5000 high-NA EUV lithography scanner. (Courtesy of ASML)

Prior to the availability of the first high-NA tool, dedicated lab equipment and current-generation EUV lithography tools and materials are being pushed to their limits to prepare and derisk the new high-NA EUV lithography technology as much as possible.

Simultaneously, imec is partnering with ASML to open a joint High-NA Lab, where a high-NA system will be linked to a coat and development track and surrounded with metrology equipment. Together, they will pioneer the ecosystem for the industry to meet the process requirements and establish the infrastructure that goes along with high-NA tool development – including anamorphic imaging, new mask technology, metrology, resist screening and materials development for thin-film patterning, etc. In addition, chipmakers will have access to the High-NA Lab to develop their private high-NA use cases.



Evolution of the reduction in resist film thickness (HP = half pitch).

Process and metrology needs

The tendency towards thinner resists (Figure 2) will continue with the advent of high-NA EUV lithography, which ultimately aims at printing lines/spaces of 16 nm pitch, corresponding to printing lines with widths as small as 8 nm. This calls for resist films thinner than 20 nm to maintain the ideal aspect ratio of 2:1 (defined as the ratio between the height and the width of the line). With thicker resists, the aspect ratio would increase, and with it the risk of line collapse.

High-NA EUV lithography brings a second reason for using thinner resist films. Following a second Rayleigh equation, the depth-of-focus (DOF) – i.e. the resist height across which the (aerial) image is in focus – decreases by the square of the numerical aperture. Simulations predict an effective decrease of DOF with a factor of 2-3 with respect to current 0.33NA lithography. A transition from thicker to thinner resists is therefore needed to cope with both a lower DOF in high-NA EUV lithography and a reasonable aspect ratio.

The reduced resist thickness requirements bring new needs for the high-NA EUV processes as well as new challenges to the metrology. For example, when the resist becomes ultrathin, the amount of material within a printed line becomes so small that it can hardly be 'seen' with the currently used metrology tools. For the widely used CD-SEM (CD scanning electron microscopy), for example, using thinner resists translates into a strongly reduced image contrast. Recent experiments revealed that the type of underlayer (i.e., the layer underneath the photoresist film) can positively affect the SEM imaging contrast. But using a different underlayer to improve the metrology will in turn impact pattern transfer, calling for optimised etch processes. To continue optimising pattern transfer, improved metrology tools or optimised tool settings will be needed to reliably image the patterns.

Below, we present a grasp of some recent insights in both patterning and metrology.

The limits of pattern transfer

In anticipation of the first high-NA EUV prototyping system, imec uses an advanced 0.33NA EUV lithography system, the NXE:3400B, to predict the performance of thinner resists – for both lines/spaces and contact holes. Earlier, imec and ASML were able to print the smallest pitch