NEXT MAJOR STEP IN LITHO – THE IMEC PERSPECTIVE

In the course of 2025, we expect to see the introduction of the first high-NA extreme ultraviolet (EUV) lithography equipment in high-volume manufacturing environments. These next-generation lithography systems will be key to advance Moore's Law towards the logic 2-nm technology generation and beyond. In this article, imec scientists and engineers involved in preparing this major next step in semiconductor lithography (driven by equipment maker ASML) discuss challenges and opportunities. They highlight recent insights and progress obtained in developing the patterning processes, metrology and photomasks needed for enabling the high-NA EUV lithography infrastructure.

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A leap in resolution

2019 marked an important milestone for extreme ultraviolet (EUV) lithography: ASML's EUV lithography systems were for the first time deployed in the mass production of logic chips of the 7-nm technology generation. Inserted to pattern the most critical layers of the chips' back-end-of-line, it enabled printing metal lines with pitches as tight as 36-40 nm.

With an extremely short wavelength of 13.5 nm, EUV lithography was introduced to succeed 193-nm (immersion) lithography as the most cost-effective manufacturing solution for the most advanced chip nodes. This transition was dictated by the Rayleigh equation for resolution: $R = k_1 \cdot \lambda / NA$, with k_1 a constant (process factor), λ the wavelength and NA the numerical aperture. According to this equation, the resolution of a lithography tool – and thus its ability to print features with a certain half pitch or critical dimension (*CD*) – can be improved by using light with smaller wavelength during wafer exposure. Moreover, the complex, expensive multiple-patterning requirements of 193 nm – which involve splitting a chip pattern into two or more simpler masks – could be moved back again to single-patterning EUV.

On the development side, researchers have been continuously trying to push further the single-print capability of today's most advanced EUV full-field scanner, ASML's NXE platform. Last year, for example, imec and ASML were able to demonstrate 28-nm-pitch single-exposure patterning readiness for lines/spaces, corresponding to critical back-end-of-line metal layers of a 5-nm logic technology node. This brings the current scanner close to its resolution limit for high-volume manufacturing, which is around 13 nm (26 nm pitch). Along with the evolution in logic, memory manufacturers are increasingly looking at using EUV lithography for meeting the high-density requirements for future memories – for example for patterning critical DRAM structures.

At the same time, multiple-patterning EUV lithography options are being explored to advance EUV to the next nodes. While these 'tricks' offer more relaxed pitches, they also come with a downside: an increased number of processing steps, adding to the cost, complexity and processing time of the patterning step.

2023 will mark a new milestone in the evolution of EUV lithography. By then, the first new generation of EUV lithography tools is expected to enter the scene: a high-NA EUV lithography scanner – projected to print the most critical features of 2-nm (and beyond) logic chips in a smaller number of patterning steps. The transition towards high-NA lithography is again justified by the Rayleigh equation, which provides a second knob for improving the resolution: increasing the *NA* of the projection lens. The *NA* controls the amount of light (more precisely, the number of diffraction orders) that is used to form the image, and thus controls the quality of the image.

Transitioning to higher-NA imaging equipment has been applied before, remember the move from 193-nm dry to 193-nm immersion lithography. At that time, the optical trick of replacing the air between lens and wafer with water allowed a 45% increase in *NA*. In the case of EUV, ASML will move from the current *NA* of 0.33 to 0.55 (i.e., a 67% increase) by redesigning the optics within the lithography system. 0.55NA EUV lithography promises to ultimately enable 8 nm resolution, corresponding to printing lines/spaces of 16 nm pitch in one single exposure.

AUTHORS' NOTE

All authors work at imec, a leading nanoelectronics research centre based in Flanders (B). Danilo De Simone is the principal staff member leading the research on patterning materials for EUV lithography, Gian Lorusso is a principal scientist working on EUV and metrology, Vicky Philipsen is a lithography engineer, and Kurt Ronse is the Advanced Patterning Program director. This article is a slightly abridged version of a longread that was published last October on the imec website.

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An ambitious timeline

0.55NA EUV lithography will push the patterning towards features smaller than what is possible with current 0.33NA EUV lithography systems. But the road forward is ambitious. The development of EUV lithography systems goes back to the 2000s, with a ten-year time span between the installation of the first pre-production EUV scanners and the recent introduction of EUV lithography in high-volume manufacturing. For high-NA, the ambition is to compress that time frame to only three years, with a first prototype (the EXE:5000; Figure 1) foreseen for 2023.


Rendering of ASML's EXE:5000 high-NA EUV lithography scanner. (Courtesy of ASML)

Prior to the availability of the first high-NA tool, dedicated lab equipment and current-generation EUV lithography tools and materials are being pushed to their limits to prepare and derisk the new high-NA EUV lithography technology as much as possible.

Simultaneously, imec is partnering with ASML to open a joint High-NA Lab, where a high-NA system will be linked to a coat and development track and surrounded with metrology equipment. Together, they will pioneer the ecosystem for the industry to meet the process requirements and establish the infrastructure that goes along with high-NA tool development – including anamorphic imaging, new mask technology, metrology, resist screening and materials development for thin-film patterning, etc. In addition, chipmakers will have access to the High-NA Lab to develop their private high-NA use cases.

Process and metrology needs

The tendency towards thinner resists (Figure 2) will continue with the advent of high-NA EUV lithography, which ultimately aims at printing lines/spaces of 16 nm pitch, corresponding to printing lines with widths as small as 8 nm. This calls for resist films thinner than 20 nm to maintain the ideal aspect ratio of 2:1 (defined as the ratio
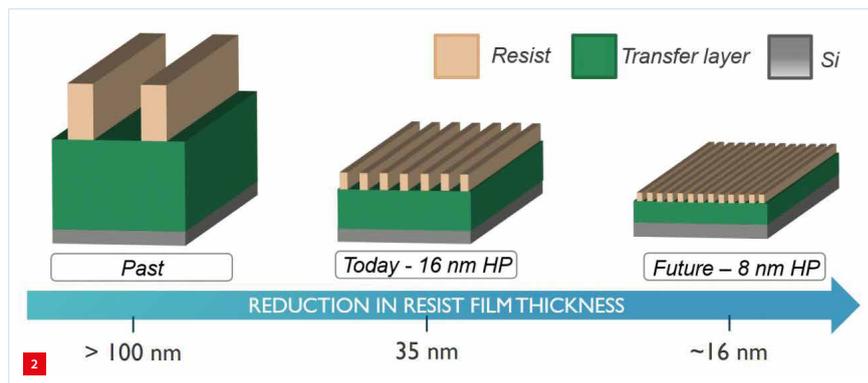
Evolution of the reduction in resist film thickness (HP = half pitch).

between the height and the width of the line). With thicker resists, the aspect ratio would increase, and with it the risk of line collapse.

High-NA EUV lithography brings a second reason for using thinner resist films. Following a second Rayleigh equation, the depth-of-focus (DOF) – i.e. the resist height across which the (aerial) image is in focus – decreases by the square of the numerical aperture. Simulations predict an effective decrease of DOF with a factor of 2-3 with respect to current 0.33NA lithography. A transition from thicker to thinner resists is therefore needed to cope with both a lower DOF in high-NA EUV lithography and a reasonable aspect ratio.

The reduced resist thickness requirements bring new needs for the high-NA EUV processes as well as new challenges to the metrology. For example, when the resist becomes ultrathin, the amount of material within a printed line becomes so small that it can hardly be 'seen' with the currently used metrology tools. For the widely used CD-SEM (CD scanning electron microscopy), for example, using thinner resists translates into a strongly reduced image contrast. Recent experiments revealed that the type of underlayer (i.e., the layer underneath the photoresist film) can positively affect the SEM imaging contrast. But using a different underlayer to improve the metrology will in turn impact pattern transfer, calling for optimised etch processes. To continue optimising pattern transfer, improved metrology tools or optimised tool settings will be needed to reliably image the patterns.

Below, we present a grasp of some recent insights in both patterning and metrology.

The limits of pattern transfer
In anticipation of the first high-NA EUV prototyping system, imec uses an advanced 0.33NA EUV lithography system, the NXE:3400B, to predict the performance of thinner resists – for both lines/spaces and contact holes. Earlier, imec and ASML were able to print the smallest pitch

possible with this NXE:3400B scanner (i.e., 24-nm pitch lines/spaces and 28-nm pitch contact holes).

By using this tool, the team showed, for example, that the line-edge and line-width roughness (LER/LWR) – among the most critical parameters for patterning lines/spaces – tend to increase when using thinner resist films. In these experiments, chemically amplified resists (CARs) were used, a type of resist that relies on chemical amplification of electrons formed within the resist when EUV photons hit the surface.

For high-NA lithography, however, the industry might need resists beyond CARs, with better resolving power. We therefore see an emergence of novel photoresist materials such as metal-oxide resists (MORs). Our first experiments seem to indicate that these MORs have indeed a better pattern transfer capability for smaller features and thinner resists. Imec collaborates with multiple material suppliers to develop these concepts and assess critical issues such as contamination risks and process integration challenges.

Metrology
Imec sees two ways to address the issue of decreasing image contrast of presently used CD-SEM tools, and to continue measuring very small lines printed with ever thinner resists. A first approach is to tweak the tool's settings. Playing with some of the knobs of the CD-SEM tool (such as the scan rate) turns out to positively affect the imaging contrast – making patterns visible even at film thicknesses down to 15 nm (Figure 3). A second approach is to explore alternative metrology techniques, in close collaboration with metrology suppliers. Very promising in terms of resolution are for example low-voltage SEM, helium-ion microscopy, and scatterometry.

Apart from lines of e.g. 10 nm width, there are even smaller features within the pattern that need to be imaged. As scaling continues, it has become more difficult to measure parameters like LER and overlay performance (i.e. how well one layer is aligned with the next one) – requiring image resolution far below 10 nm.

And then there is defectivity, more particularly, the appearance of stochastic print failures: random, non-repeating, isolated defects such as microbridges, locally broken lines and missing or merging contacts. They are believed to arise from the fundamental relationship between energy and wavelength. With the wavelength getting shorter, the energy from the light source is distributed over less photons. Consequently, there are just a few photons to create a pattern. Besides this 'photon shot-noise effect', stochastic effects originate from the molecular nature of matter, and the probabilistic behaviour of their interactions.

The advent of high-NA EUV lithography with further increasing resolution and reduced resist thicknesses will further drive this evolution. Imec and ASML have been developing methodologies to systematically quantify the defect levels in the EUV materials and learn about the many factors contributing to the failures. Key is the development and improvement in wafer inspection strategies, which traditionally rely on optical techniques.

More recently, e-beam based inspection is gaining increased attention. Although it looks very promising for finding small defects, it comes with a major drawback: a dramatic increase of the time needed for inspecting the full wafer – calling for solutions for enhanced tool productivity and throughput. Meanwhile, ASML is working on a fast multi-beam inspection tool that leverages several of ASML's core technologies: advanced stages, computational technology and advanced electron optics.

Besides, electrical tests of metallised patterns are increasingly being set up to look for correlations with data obtained with optical and e-beam inspection techniques. This allows to increase learnings on stochastic patterning failures and to gain more insights in the way they impact yield.

Mask technology
The photomask is an essential component for the manufacturing of chips as it holds the design layout information intended for the final device. Ideally, this information is contained in dark (i.e., absorbing) and bright (i.e., reflecting) areas on the mask. Now that progressively
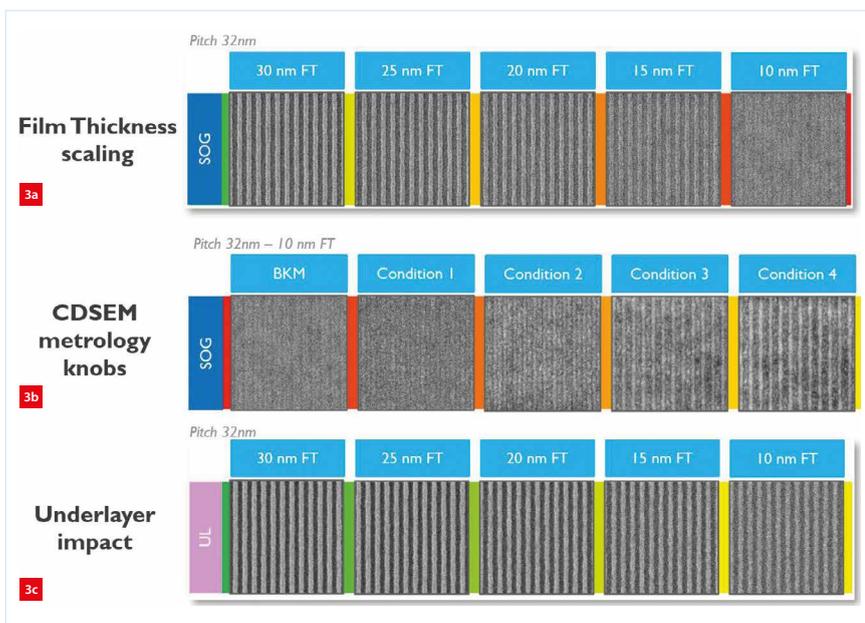
Impact of reducing the resist film thickness (from 30 to 10 nm) on the CD-SEM image contrast.
(a) Negative effect.
(b) Improvement by playing with CD-SEM metrology knobs.
(c) Improvement by using different underlayers.

smaller features are being printed, deviations from the ideal mask are increasingly impacting the final wafer pattern. Mask-specific challenges therefore need to be addressed. These include, amongst others, a reduction of the mask 3D effects, an enhanced understanding of the mask lifetime and of its contribution to printing stochastic failures. On top of that, the introduction of anamorphicity (see below) within the high-NA EUVL optical system brings along additional complexities to the mask industry.

In close collaboration with ASML and with its material suppliers, imec contributes to the design optimisation and qualification of photomasks intended for high-NA EUV lithography. This work is described in more detail below.

New absorber materials
Today's EUV photomasks consist of a ~300-nm-thick reflective multilayer stack, formed by 40 to 50 alternating layers of silicon (Si) and molybdenum (Mo), capped with a thin ruthenium layer. On this stack, the absorber made of tantalum-boron-nitrate (TaBN) carries the pattern. While the multilayer of Mo and Si reflects the incident light, the absorber blocks the reflection and this combination defines the features on the wafer.

Current Ta-based absorbers are typically about 60-70 nm thick, designed to absorb a sufficient amount of light. This thickness is large compared to the 13.5-nm exposure wavelength of the light. Consequently, light that hits the mask under a certain angle of incidence (centred around 6° in conventional EUV lithography) and reflects from the multilayer is sensitive to the 3D topography of the 'thick' mask, undergoing for example multilayer- and absorber-induced phase deformations. This distorts the aerial image – the pattern of light that finally is transferred in the photoresist – and reduces its image contrast. These so-called mask 3D effects also come with increased feature-dependent variations in placement and best focus on the wafer. This presents additional challenges for high-NA EUV lithography, that already suffers from a reduced DOF budget.

Originally, innovations in source illumination and mask design were applied to compensate for the mask 3D effects. In recent years, attention is shifting towards improving the mask material as the parameter to control mask 3D effects on the wafer and thus help to increase high-NA DOF. This has driven imec's research into exploring new absorber materials, that either have a different EUV refractive index (low-n materials such as RuTa or PtMo allowing for attenuated phase shifting) or a high EUV extinction coefficient (high-k materials such as PtTe or Ni with high absorbing capability). For each of the material types, thickness optimisation is required to give the best imaging trade-off.
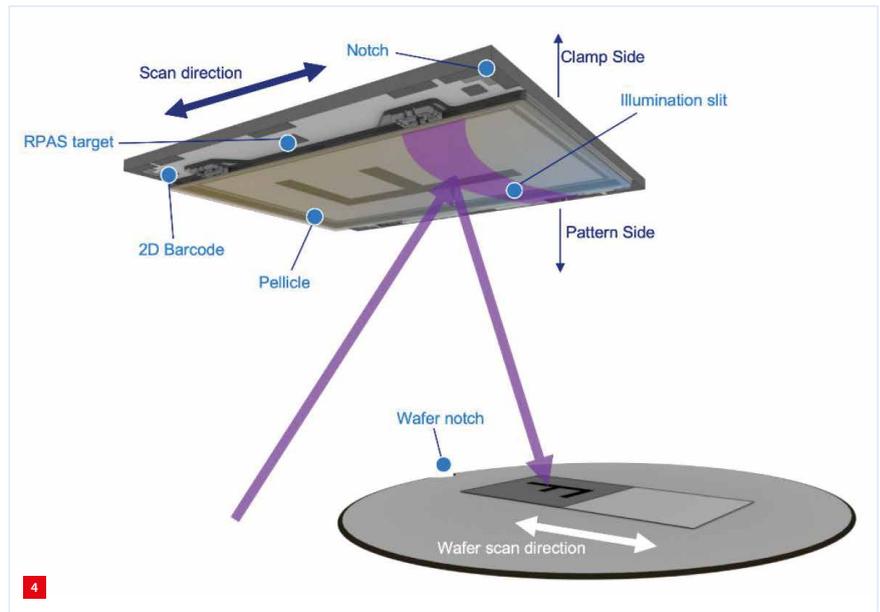
Schematic representation of an anamorphic mask, and main orientations of mask and wafer during printing on a 0.55NA scanner. (Courtesy of ASML)

Anamorphicity
High-NA EUV lithography comes with a significant redesign of the optics within the scanner, allowing light with larger angles of incidence to hit the wafer – giving the system a higher resolution. At equal scanner magnification (actually, demagnification), this would come with a drawback. Light with higher angles of incidence will hit the mask as well and, without action, this would dramatically worsen the 3D mask effects.

One approach to overcome these additional shadowing effects would be to increase the mask magnification from its historical 4x to 8x, in combination with using larger mask blanks. But abandoning the original 6-inch x 6-inch mask dimensions while preserving a high mask quality would dramatically impact the mask industry.

To minimise that impact, ASML and Zeiss have introduced anamorphic optics, with different magnification in the x- and y-directions (4x and 8y (y being the scanning direction), respectively). The 6-inch mask is preserved, but its design is stretched in one direction (Figure 4). The increased magnification (in one direction) cuts the image field size (i.e., the part of the wafer that is exposed in one step) to one half, so the scanner may end up printing the features on only part of the device. This is especially true for chips with larger die sizes, imposing a constraint on how these chips need to be designed.

For the chips with larger die sizes, chipmakers must resort to a technique called stitching. One part of the pattern is exposed with one mask, the next part with a second mask,

and the two masks are stitched together. Imec investigates methods for improved stitching, for example by reducing the so-called transition zone that inherently exists between both masks. On the hardware side, ASML has worked towards accelerated mask and wafer stages to compensate for the loss of productivity caused by the half-field imaging.

Pellicle development
In lithography, the photomask is usually mentioned in the same breath with the pellicle – the membrane used to protect the mask from contamination during high-volume semiconductor manufacturing. It is mounted a few millimeters above the surface of the photomask so that if particles land on the pellicle, they will be too far out of focus to print.

Developing an EUV pellicle is however not straightforward. A major challenge generic to all EUV scanners is to make the pellicle absorb as little as possible to maintain the throughput and economics of EUV lithography. In addition, the pellicle must be able to survive exposure to the increasing EUV power of future lithography tools, including the high-NA EUV lithography tools – for which the 8x magnification comes with the benefit of reduced power density on pellicle and mask level.

ASML has engineered a pellicle with 90% transmission, which can handle 380 W source power and is fully compatible between the low-NA and high-NA platforms. While imec, in collaboration with its partners, has developed an innovative CNT-based pellicle solution (Figure 5) that has potential to survive scanner powers beyond 600 W. The CNT (carbon nanotube) pellicle feasibility was already successfully demonstrated through use on the EUV NXE:3300 scanner at imec. The team is now working to extend the lifetime to enable a high-productivity pellicle solution suitable for next-generation

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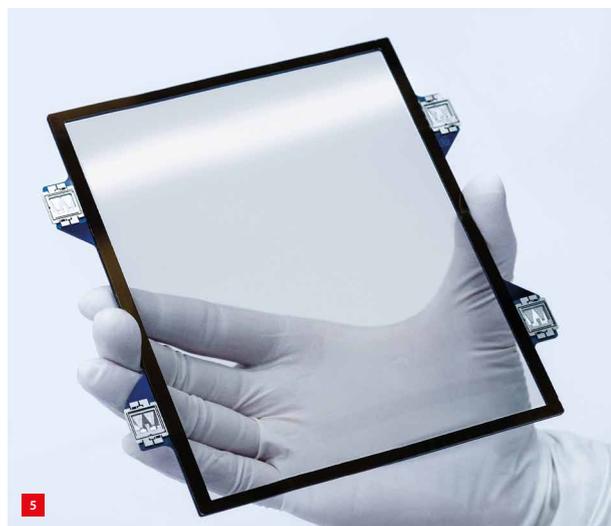
A full-sized CNT-based pellicle similar to those exposed in imec's NXE:3300B.

EUV lithography tools, including high-NA, with its strongly increased reticle acceleration.

More mask issues
The imec team also focuses on other mask-specific issues, such as mask lifetime. Masks are subject to carbon growth when stored, and this affects the critical dimension of features printed on the wafer. The effect is observed to depend on the storage conditions and can be reversed by EUV exposure.

Another challenge relates to the increasing contribution of mask deficiencies to the stochastic failure probability. The surface roughening of the mask's multilayer, which increases with mask ageing, is observed to play a crucial role. This drives the research of alternative multilayer 'mirror' materials. In addition, more than before, small mask imperfections translate into errors observed after wafer printing, as a direct consequence of scaling. All this urges the need for massively quantifying the mask contribution to the wafer imaging performance.

In addition, other methods for writing the masks with more precision and smaller resolution are being investigated, including multibeam mask writing, which allows for different (so-called curvilinear) mask shapes.

AttoLab
The need for speeding up learnings on thin-resist imaging was one of the reasons why imec decided to invest in AttoLab, a joint project with US-based KMLabs. The lab allows us to explore the fundamental dynamics of photoresist imaging under high-NA EUV lithography conditions before the first 0.55NA EXE:5000 prototype from ASML becomes available. Within the AttoLab, the high-NA exposure at 13.5 nm is emulated with a bright, coherent, high-harmonic EUV source in an interference-type of set-up.

Recently, with a Lloyd's-Mirror-based interference set-up for coupon (test specimen) experiments (Figure 6), 20-nm pitch lines/spaces could for the first time be successfully imaged at imec in a metal-oxide resist. In this arrangement, light reflected from a mirror interferes with light directly emitted by the 13.5-nm high-harmonic source, generating a finely detailed interference pattern suited for resist imaging. The pitch of the imaged resist pattern can be tuned by changing the angle between the interfering light beams. This set-up supplies the critical learnings for the next step: expansion to a 300-mm wafer interference exposure that theoretically can go down to an unprecedented 8 nm pitch.

While ASML's scanners are designed for mass production of chips, the interference type of tools as used in the AttoLab will never achieve the required full-field through-

put. But with these 13.5-nm femtosecond-enveloped attosecond laser pulses, imec is pursuing a different goal, i.e., using a variety of techniques, to study EUV photon absorption and ultrafast radiative processes that are subsequently induced in the photoresist material, and learn more about the critical stochastic print failures.

Conclusion

The move to high-NA EUV lithography presents a major opportunity for the lithography community to jointly tackle the challenges and to prepare for the tool's introduction in only a very short time frame. Together with ASML in a joint High-NA EUV Lab, imec is focusing on the infrastructure preparation that comes along with high-NA scanner development. For that purpose, imec is relying on and invites all material and equipment suppliers to contribute to the establishment of a complete high-NA ecosystem. The reward for all these efforts will be big, as the 0.55NA EUV lithography tool promises to advance Moore's Law towards 2-nm technology generations and beyond.

Acknowledgements
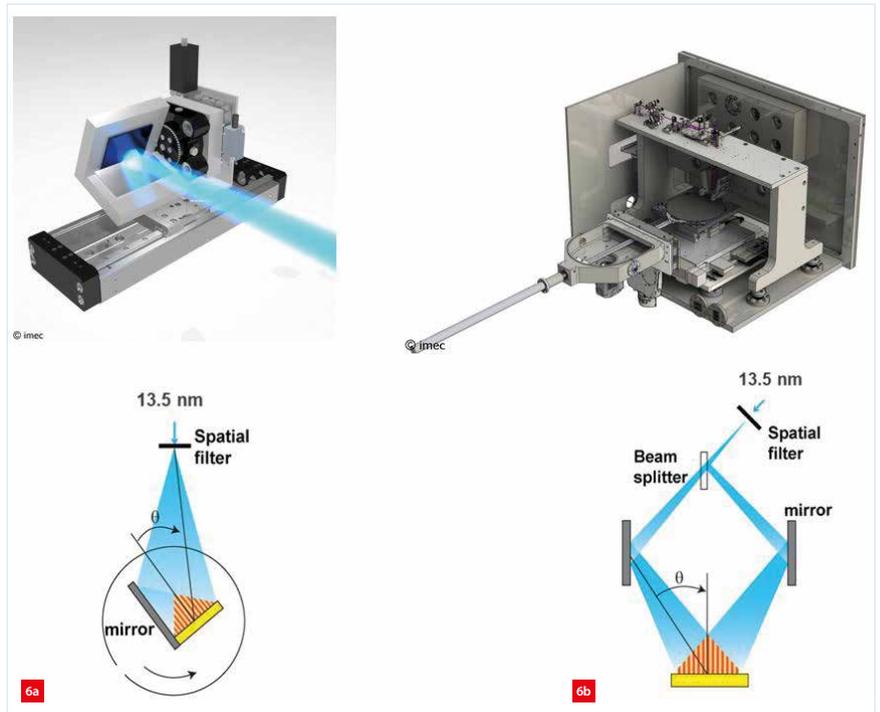
Schematic representations (not to scale) of AttoLab measurement set-ups.
(a) Lloyd's Mirror set-up for high-NA EUV interference coupon experiments.
(b) Interference chamber for full 300-mm wafer experiments.