A breakthrough

Photonic Integrated Circuits, also called optical chips or PICs, are considered as the way to make photonic systems or subsystems cheap and ubiquitous. However, PICs still are several orders of magnitude more expensive than their microelectronic counterparts, which has restricted their application to a few niche markets. Recently, a novel approach in photonic integration has emerged to reduce the R&D costs of PICs by more than a factor of ten. It will bring the application of PICs that integrate complex and advanced photonic functionality on a single chip within reach for a large number of small and larger companies. Europe is leading in this novel approach and the Netherlands is playing a key role.

Meint Smit

Figure 1 shows the complexity development of optical chips for application in Wavelength Division Multiplexing (WDM) in telecommunication systems, the technology that enabled worldwide high-speed internet and that is a major driver for photonic integration. The complexity is measured

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Figure 1. The complexity development of photonic ICs for WDM applications (red points reported by Dutch groups).

as the number of optical components per chip [1] [2]. Figure 2 shows an early example of such a chip. The most complex chip reported today is a WDM transmitter chip that integrates 40 wavelength channels, each of them containing a laser, a modulator, a power monitor and a channel equalizer [3].



Figure 2. An optical crossconnect (OXC) chip that can switch four wavelength channels independently from two input waveguides to two output guides. It integrates two

wavelength demultiplexers with 16 optical switches on a chip area of $8x12 \text{ mm}^2$ (the point labeled 'Herben99' in Figure 1).

in photonic integration

Moore's law

Figure 1 shows a clear exponential trend in the complexity development for photonic ICs, similar to Moore's law in electronics (which 'predicts/describes' the complexity of electronic ICs doubling each 18 months). The figure suggests that photonics is following the process-driven development of microelectronics, albeit at a slower pace and with a 30 years time shift. There is an important difference, however: the well-known Intel plot is about commercially applied devices, whereas most of the points in Figure 1 are research results which did not bring it to the market. The only chip currently applied in a commercial product is the WDM transmitter chip (10x10 Gb/s) of the US-based company Infinera (labeled Nagarajan05 in Figure 1). It is used in a 100 Gb/s WDM system that is proving to be very competitive, and it is the first demonstration that complex PICs provide a competitive edge.

What went wrong?

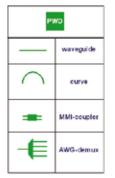
Why have so few of the advanced PICs reported in the literature made it to the market, despite the fact that in the last two decades several billion dollars have been invested worldwide in development of integration technologies? The main reason is that they are too expensive to compete with technologies like micro-optic or hybrid integration. The problem with current project funding models within Europe is that they tie the technology development closely to an application: no money without a clear and challenging application. Hence the technology has to be fully optimized for that application and, as a result, we have almost as many technologies as applications. Due to this huge fragmentation the market for these specific technologies is usually too small to justify their further development into the industrial volume manufacturing process that would really lead to low chip costs. The few that made it suffer from small profit margins, if any. This is quite different from the situation in microelectronics where a huge market is served by a relatively small set of integration (CMOS) technologies, and development costs of the integration process are shared by a large number of (large-volume) applications.

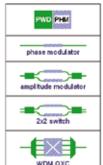
Generic integration technology

The solution seems obvious, following the microelectronics approach: developing low-cost Application Specific Photonic ICs (ASPICs) in *generic integration* technologies that can serve a wide variety of applications and have much better market perspectives. In microelectronics a broad range of functionalities is realised from a rather small set of basic building blocks, like transistors, diodes, resistors, capacitors and interconnection tracks. By connecting these building blocks in different numbers and topologies we can realize a huge variety of circuits and systems, with complexities ranging from a few hundred up to over a billion transistors.

In photonics we can actually do something similar. Most optical circuits consist of a rather small set of components: lasers, optical amplifiers, modulators, detectors and passive components like couplers, filters and (de)multiplexers. By proper design these components can be reduced to an even smaller set of basic building blocks. In a generic integration technology that supports integration of the basic building blocks we can realize a variety of functionalities.

Figure 3 illustrates which functionalities can be realised in a generic Indium Phosphide technology that supports integration of three basic building blocks: passive waveguide devices (PWD), phase modulators (PHM) and semiconductor optical amplifiers (SOA). With these a variety of modulators, switches and lasers can be realised. Figure 4, for example, shows an integrated discretely tunable laser with nanosecond switching speed, useful for packet switching applications, which has recently been developed in a generic technology by the COBRA research





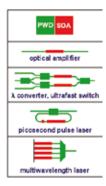
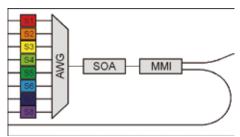


Figure 3. Examples of the functionalities that can be realised in a generic integration technology that supports three basic building blocks: passive waveguide devices (PWD), (optical) phase modulators (PHM), and semiconductor optical amplifiers (SOA).



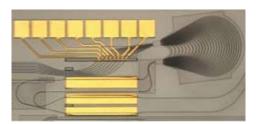


Figure 4. Circuit scheme and microscope photograph of a fast discretely tunable laser with 100 GHz channel spacing, which has recently been realised in the COBRA InP-based generic integration process. Chip dimensions are $1.5 \times 3.5 \text{ mm}^2$.

institute in Eindhoven. The schematic on the left shows how the laser is composed of only two basic building blocks: PWDs in the MMI-coupler, the arrayed-waveguide grating (AWG) demultiplexer and the interconnections, and SOAs for amplification and switching.

An advantage of generic integration technologies is that, because they can serve a large market, they justify the investments in developing the technology for a very high performance at the level of the basic building blocks, which will make circuits realised in this technology highly competitive. This performance will not apply for every application, of course. Just like in CMOS different classes of applications need different processes, e.g. for highvoltage, high-power or low-power, high-speed etc. In a similar way, generic photonic processes will need a few different generic technologies, optimized for different kinds of applications, to cover a major part of all applications. In a fully-fledged generic integration technology we will need a few additional building blocks, like polarisation converters for on-chip handling and control of polarisation, DBR gratings as on-chip reflectors, and fibre mode adapters for low-loss coupling to fibres. And we might also want a process with compact electroabsorption modulators instead of the longer phase modulators. But the number of basic building blocks will remain pretty small, and the number of generic technologies required is far smaller than the number of technologies which are presently in use.

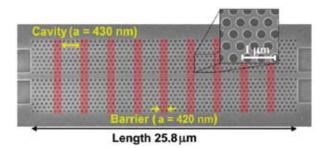
Today, several companies in Europe have integration processes that are suitable as a starting point for development of a truly generic integration process. What still is missing, is the organizational and software infrastructure to provide easy and low-cost access.

A foundry approach

In September 2004, the European Network of Excellence on Photonic Integrated Components and Circuits, ePIXnet, started with a healthy mix of academic and industrial partners on an ambitious mission: to move from a model of independent research to a model of integrated research with shared use of expensive technological infrastructure, such as cleanroom facilities. The idea was to stimulate cleanroom owners to organise access to their facilities for a broader circle of non-cleanroom owning partners.

Next, ePIXnet took the step to the foundation of integration technology platforms. Two major integration technologies were identified: InP-based, supporting the highest degree of functionality, including compact lasers and amplifiers, and silicon photonics technology, offering most of the functionality offered by InP except for the compact lasers and amplifiers, but at a potentially better performance and lower cost because of its compatibility with mature CMOS technology; see Figure 5. For both technologies a platform organization was established. Later a third platform with dielectric waveguide technology was added, offering lowloss and high-quality passive optical functions and some thermo-optic active functions, through the whole wavelength range from visible to infrared. In addition to these three integration platforms, ePIXnet established four supporting platforms: for nanolithography, packaging, high-speed characterization, and massive cluster computing. Now, early 2009, we may conclude that ePIXnet activities will survive after the expiration of EU network funding by the end of 2008.

The Silicon Photonics platform is presently supported by Europe's major CMOS research institutes IMEC and LETI and coordinated by the University of Ghent (Belgium). It



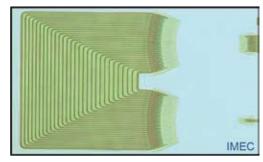


Figure 5. Examples of circuits realised in the ePIXfab silicon-on-insulator technology platform: a complex photonic crystal waveguide filter with a periodically changing lattice constant (left) and an extremely compact 8-channel AWG demultiplexer with high performance.

offers low-cost shared access to processes for high quality silicon photonic ICs to an increasing number of customers, also from outside Europe.

The InP-based technology platform is supported by a consortium containing Europe's key players in the field of InP-technology: chip manufacturers, photonic CAD companies, equipment manufacturers and research institutes. It is coordinated by Eindhoven University of Technology. Within the framework of an EU project and a Dutch national project it is working on the development of industrial generic foundry capability, including software design kits for fast and accurate chip design, and generic packaging and test facilities. Commercial photonic foundry operation is projected in 2013. Restricted access to alpha and beta versions may start as early as 2011. Until that time the COBRA research institute in Eindhoven will provide small-scale access to its generic integration process, for research purposes (proof-of-concept, example in Figure 4).

The third platform, which is supported by the Dutch company Lionix and the University of Twente, provides access to its flexible Triplex dielectric (glass) waveguide technology (SiO_2 and Si_3N_4); see Figure 6. Also the four supporting platforms are rapidly broadening their user base outside the ePIXnet network, gradually moving to full user funding.

The generic integration approach adopted by the ePIXnet platforms is expected to lead to a dramatic cost reduction in both PIC R&D and manufacturing, and a significant reduction of the number of design cycles needed to come to a satisfactory device, mainly because these platforms offer access to a well-characterized process, rather than to a cleanroom. A breakthrough is expected to happen in the next few years. And, due to cooperation that was initiated in ePIXnet, it will most probably start in Europe. Although the ideas about foundry operation have been developed in close cooperation with the organization of the US optoelectronics industry OIDA, Europe clearly has a head start in this novel approach to Photonic IC R&D and manufacturing.

Applications

Consequently, this cost reduction will lead to a large growth of PICs market share. So far, the use of PICs has been mainly restricted to some niche areas in high-end telecom applications. Now, they will also become competitive in high-volume markets like the telecom access network.

But when chip costs drop photonic chips will increasingly penetrate other applications, as in fibre sensors. A significant part of sensor costs is in the readout unit, which contains a light source, a detector and some signal



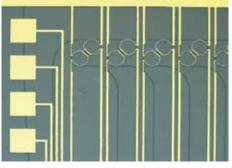


Figure 6. Two examples of ASPICs realised in the Triplex generic technology platform: a photonic true-time delay system for microwave phased arrays antennas (left) and an integrated optical add-drop multiplexer (right).

processing circuitry. Here PICs can replace a significant part of existing modules, and enable novel sensor principles (regarding for example strain, heat or chemical signals).

Another interesting class of devices are pico- or femtosecond pulse lasers. Here PICs containing mode-locked lasers, optionally combined with pulse shapers, can provide small and cheap devices that can be used in widely differing applications, such as high-speed pulse generators and clock recovery circuits, ultrafast AD converters, and multi-photon microscopy.

Once ASPICs and their development get really cheap they will enter into many advanced products. This offers ample opportunities to small and larger companies for applying ASPICs in their products.

Roadmap

The microelectronics roadmap is focused on progress along the Moore's law curve. In photonics, a different development may be expected. It will start with commercial application of ASPICs with a complexity in the range of 5-50 components in rather basic generic foundry processes. The next step will be an increase in performance and capabilities of the generic processes, e.g. with respect to speed, power consumption and number of basic building blocks supported, which may lead to some – but no dramatic – increase in the complexity of the chips. Once the foundry processes cover a wide range of applications, their steady performance improvement will allow for designing increasingly complex chips.

However, it may not be expected that the complexity supported by the generic processes as described here will exceed a component count of 1,000, for a number of reasons. Firstly, SOAs and lasers typically have a power dissipation of several 100 mW. So their number is typically restricted to several tens up to a maximum of a few hundreds, because of heat sinking limitations. Secondly, although they often carry digitally modulated signals, the basic building blocks and the circuits built from them essentially operate in an analog mode, which means that on passing a number of components the signal will accumulate noise and distortion and needs to be regenerated. Regenerators can be integrated too, but they consume space and power.

Finally, from a functionality point of view it is difficult to imagine what circuits would need more than a thousand components. In micro-electronics, the breakthrough to VLSI did not occur in analog electronics but in digital electronics, where signal regeneration inherently occurs after each processing step, so that operations can be concatenated endlessly.

Digital photonics

For photonic integration to move towards (V)LSI circuit complexity a change from analog to digital signal processing will be necessary too. Especially digital photonics based on coupled micro- or nanolasers is a promising candidate for integrating large numbers of digital circuits. It is not obvious, however, that digital photonics will become as successful as digital electronics, because it abandons a lot of the advantages of light, such as the design freedom offered by the wavelength dimension, and in all-optical signal processing the absence of electrical charge which limits operation speeds. And in digital applications it has to compete with electronics 'at its best', in digital signal processing.

Yet, the situation for digital photonics is not hopeless. The recent breakthrough in plasmonic lasers [4] [5], which are not larger than modern transistors and can operate with low switching energies at very high switching speeds, holds the promise that digital photonic circuits with more than 100,000 lasers operating at THz clock rate, will become reality. Such circuits might avoid a lot of power-hungry electro-optical conversions in high-speed internet routers. And they might bring photonic integration three decades further on the Moore's law curve. But this will take many years. The first thing to happen is the breakthrough of 'analog' generic photonic foundry technology. And in Europe this may happen pretty soon.

Author's note

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References

- [1] R. P. Nagarajan and M.K. Smit, "Photonic integration", *IEEE LEOS Newsletter* Vol 21, Nr. 3, June 2007, pp. 4-10.
- [2] M.K. Smit and C. Van Dam, "PHASAR-based WDM devices: principles, design and applications", *J. of Sel. Topics in Quantum Electron.*, Vol. 2, No. 2, June 1996, pp. 236-250.
- [3] R. Nagarajan et al., "Large-scale photonic integrated circuits for long haul transmission and switching", *J. Opt. Networking*, Vol. 6, No. 2, Feb. 2007, pp. 102-111.
- [4] M. T. Hill et al, "Lasing in Metallic-Coated Nanocavities", *Nature Photonics*, Vol. 1, pp. 589-594, 2007
- [5] F. Zuurveen, "Metal-coated nano-cavity laser", *Mikroniek*, Vol. 48, No. 3, June 2008, pp. 34-36.

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